



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

10/563,717

01/06/2006

Stefan Muller

PD030074

1519

24498

7590

10/27/2008

Joseph J. Laks

Thomson Licensing LLC

2 Independence Way, Patent Operations

PO Box 5312

PRINCETON, NJ 08543

EXAMINER

ALPHONSE, FRITZ

ART UNIT

PAPER NUMBER

2112

MAIL DATE

DELIVERY MODE

10/27/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

| | | | |
|------------------------------|--------------------------------------|--------------------------------------|--|
| Office Action Summary | Application No. 10/563,717 | Applicant(s) MULLER ET AL. | |
| | Examiner FRITZ ALPHONSE | Art Unit 2112 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 July 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 10 is/are rejected.
- 7) ☒ Claim(s) 9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office Action is in response to the amendment filed on 7/28/2008. Claims 1-10 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-8, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Demura (US Pub. No. 20020099996) in view of Greenblat (US Pub. No. 20030212830) and further in view of Yuan (U.S. Pat. No. 6,526,477).

As to claim 8, Demura (figs. 1-12) show a device for error correction of an encoded data stream, including: an input buffer (figure 3, component 2) for saving the demodulated data stream (paragraph [0031]); an external DRAM to which the data are transferred after correction (paragraph [0044]); an embedded SRAM (figure 5 component 13) for performing a multipass correction on the corrected data;

Demura does not explicitly disclose “means for copying the data frame from the external DRAM to the embedded SRAM; and means for copying the corrected data back from the embedded SRAM to the external DRAM after the multipass correction.”

However, the limitations are obvious and well known in the art, as evidenced by Greenblat (paragraph [0413]). Greenblat teaches means for copying the data frame from the

Art Unit: 2112

external DRAM to the embedded SRAM; and means for copying the corrected data back from the embedded SRAM to the external DRAM after the multipass correction.

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention, to improve upon the communication system, as disclosed by Greenblat. Doing so would provide a highly robust programmable packet processor that can support a variety of high end applications, that is capable of handling a variety of protocols, and that provides desired performance in terms of speed and power.

In addition, as to claim 8, Demura does not explicitly disclose an input buffer for performing a correction process on-the-fly. However, the limitation is disclosed by Yuan (col. 8, lines 42-52).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention, to improve upon the memory device, as disclosed by Yuan. Doing so would provide a low-cost host-memory based RAID system.

As to claim 1, Demura (figs. 1-12) show a method for error correction of an encoded data stream including the steps of: saving the demodulated data stream in an input buffer (figure 3, component 2 shows an input buffer for saving the demodulated data stream) (paragraph [0031]); transferring the data to an external DRAM after correction (paragraph [0044]).

Demura does not explicitly disclose “copying the data from the external DRAM to an embedded SRAM; starting a multipass correction in the embedded SRAM; and copying the corrected data back from the embedded SRAM to the external DRAM after the multipass correction.”

Art Unit: 2112

However, the limitations are obvious and well known in the art, as evidenced by Greenblat (paragraph [0413]). Greenblat teaches means for copying the data frame from the external DRAM to the embedded SRAM; and means for copying the corrected data back from the embedded SRAM to the external DRAM after the multipass correction.

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention, to improve upon the communication system, as disclosed by Greenblat. Doing so would provide a highly robust programmable packet processor that can support a variety of high end applications, that is capable of handling a variety of protocols, and that provides desired performance in terms of speed and power.

Demura does not explicitly disclose performing a first correction process on-the-fly in the input buffer. However, the limitation is disclosed by Yuan (col. 8, lines 42-52).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention, to improve upon the memory device, as disclosed by Yuan. Doing so would provide a low-cost host-memory based RAID system.

As to claims 2-7, the dependent claims 2-7 included in the statement of rejection but not specifically addressed in the body of the rejection have inherited the deficiencies of the parent claim 1 and have not resolved the deficiencies. Therefore, they are rejected based on the same rationale as applied to the parent claim above.

As to claim 10, the claim has substantially the limitations of claim 1; therefore, they are analyzed as previously discussed in claim 1 above.

Allowable Subject Matter

4. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 9 contains allowable subject matter because none of the cited references either singular or in combination discloses “a device including a deinterleaver for deinterleaving and/or for correcting streaming discontinuities in the external DRAM.”

Response to Arguments

5. Applicant's arguments filed on 7/28/2008 have been fully considered but they are not persuasive.

Applicant argues that “In this way, the number of random accesses to the external DRAM is reduced. After gathering a full ECC block in the DRAM, the data is streamed to the embedded internal SRAM where the ECC block is corrected via multipass correction, and streamed back to the DRAM. The size of the internal SRAM is reduced. The internal SRAM correction simplifies the hardware complexity during the correction process and the overall correction process is speed up (see Specification page 2, lines 17-32). These features are neither disclosed nor suggested by the prior art.”

The examiner respectfully disagrees because some of the limitations cited in this argument “After gathering a full ECC block in the DRAM, the data is streamed to the embedded internal SRAM where the ECC block is corrected via multipass correction, and streamed back to the DRAM. The size of the internal SRAM is reduced...” are not in the claim.

Art Unit: 2112

Applicant argues that “The data are not corrected in the SRAM, but in the DRAM based on the dense maps stored in the SRAM”. Thus, Demura neither discloses nor suggests "performing a first correction process on-the-fly in the input buffer" as recited in the present claimed arrangement.

The examiner asserts that Demura does not explicitly disclose an input buffer for performing a correction process on-the-fly. However, the limitation is disclosed by Yuan (col. 8, lines 42-52). In addition, Demura (fig. 5) shows a SRAM (buffer memory 13) for correcting data.

Applicant argues that “Greenblat, similarly to Demura, also neither discloses nor suggests starting a multipass correction in the embedded SRAM...”

The examiner respectfully disagrees because Demura (figure 5 component 13) shows an embedded SRAM for performing a multipass correction on a corrected data.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

Art Unit: 2112

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz Alphonse, whose telephone number is (571) 272-3813. The examiner can normally be reached on M-F, 8:30-6:00, Alt. Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3824

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/FA/

Examiner, Art Unit 2112

October 20, 2008

/JACQUES H LOUIS-JACQUES/

Application/Control Number: 10/563,717

Page 8

Art Unit: 2112

Supervisory Patent Examiner, Art Unit 2100